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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/029,608	05/15/98	FUKASAWA	N 980233

MMC2/1020
ARMSTRONG WESTERMAN HATTORI MCLELAND & NAUGHTON
1725 K STREET NW
SUITE 1000
WASHINGTON DC 20006

EXAMINER	
GRAYBILL, D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/20/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/029,608	Applicant(s) Fukusawa et al.
	Examiner David E. Graybill	Group Art Unit 2814

☒ Responsive to communication(s) filed on *7 Aug 1900*.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *18, 19, 36, 41-43, 54-64, 70-77, 79-85, 87-91, and 95-107* is/are pending in the application.

Of the above, claim(s) *103-107* is/are withdrawn from consideration.

☒ Claim(s) *70, 72-77, 80, 84, 85, 95, and 96* is/are allowed.

☒ Claim(s) *18, 19, 36, 41-43, 54-64, 71, 79, 81-83, 87-91, and 97-102* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *20*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

The amendment to the claims filed 8-7-00 is non-responsive to the Office action filed 5-8-00 because it fails to conform to the provisions of MPEP 714.03:

714.03 Amendments Not Fully Responsive - Action To Be Taken:

> Where a bona fide response to an examiner's action is filed before the expiration of a permissible period, but through an apparent oversight or inadvertence some point necessary to a complete response has been omitted - such as an amendment or argument as to one or two of several claims involved or signature to the amendment - the examiner, as soon as he or she notes the omission, should require the applicant to complete his or her response within a specified time limit (usually one month) if the period for response has already expired or insufficient time is left to take action before the expiration of the period. If this is done the application should not be held abandoned even though the prescribed period has expired.

Specifically, in claims 97 and 98, the rejection directed to the term "the sealing resin" has not been addressed, and in claim 100, the rejection directed to the term "the ends of the protruding electrodes" has not been addressed.

Because the response appears to be bona fide, but through an apparent oversight or inadvertence the response is incomplete, and in order to continue to afford applicant the benefit of compact prosecution, the requirement to complete the response within a one month time limit is waived, the amendment is entered, and the claims are examined on the merits.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 58, 63, 64, 97, 98 and 100 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following lack sufficient literal antecedent basis:

Claims 58, 63 and 64 "the semiconductor element";

Claims 97 and 98 "the sealing resin";

Claim 100 "the ends of the protruding electrodes," and, "when the protruding electrode is exposed."

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 18, 19, 36, 42, 43, 57-64, 71, 87-91 and 97-101 are rejected under 35 U.S.C. 102(e) as being anticipated by Kata (5897337).

At column 4, line 7 to column 14, line 50 Kata teaches:

18. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 44 are formed; and a compressed resin layer 43 which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes.

19. The semiconductor device as claimed in claim 18, further comprising a heat radiating member 46 provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

36. A semiconductor device comprising: a semiconductor element having a surface on which external connection electrodes 44 are provided which are to be electrically connected to external terminals; and a resin layer 43 provided on the surface of the semiconductor element so as to cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the resin layer.

42. A semiconductor device comprising: a semiconductor element having protruding electrodes 44 formed on a surface thereof; a first compressed resin layer 43 that is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and a second compressed resin layer 46 provided so as to cover at least a back surface of the semiconductor element.

43. A semiconductor device comprising: a semiconductor element having protruding electrodes 44 formed on a surface thereof; a compressed resin layer 43 which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and external connection protruding electrodes 44 provided to the ends of the protruding electrodes exposed from the resin layer.

57. A semiconductor device comprising: a plurality of semiconductor elements 41; a compressed sealing resin 43 which seals partially or totally the semiconductor elements; and an electrode plate 60' which is provided in the compressed sealing resin and is electrically connected to the semiconductor elements, the electrode plate having portions 62' which are exposed from side surfaces of the compressed sealing resin and function as external connection electrodes.

58. The semiconductor device as claimed in claim 57, wherein the semiconductor element or elements are connected to the electrode plate in a flip-chip bonding formation.

59. The semiconductor device as claimed in claim 57, wherein the electrode plate is exposed from a bottom surface of the sealing resin in addition to the side surfaces thereof, so that portions 62' of the electrode plates exposed from the bottom surface function as external connection terminals.

60. The semiconductor device as claimed in claim 57, wherein protruding terminals 71-1 are provided to the electrode plate, and are exposed from a bottom surface of the sealing resin, so that the protruding terminals function as external connection terminals.

61. The semiconductor device as claimed in claim 60, wherein the protruding terminals are portions of the electrode plate defined by plastic deformation.

62. The semiconductor device as claimed in claim 60, wherein the protruding terminals are protruding electrodes arranged to the electrode plate.

63. The semiconductor device as claimed in claim 57, wherein the semiconductor element or elements are partially exposed from the sealing resin.

64. The semiconductor device as claimed in claim 57, further comprising a heat radiating member 60' in a position close to the semiconductor element or elements.

71. A mounting arrangement for mounting a semiconductor device on a mounting board, the semiconductor device comprising: a plurality of semiconductor elements 41; a compressed sealing resin 43 which seals partially or totally the semiconductor elements; an electrode plate 60' which is

provided in the sealing resin and is electrically connected to the semiconductor elements, the electrode plate having portions 62' which are exposed from side surfaces of the compressed sealing resin and function as external connection electrodes: and protruding terminals 67 provided to the electrode plate, and exposed from a bottom surface of the compressed sealing resin, so that protruding terminals function as external connection terminals; the mounting arrangement comprising: bumps 67 arranged to the protruding terminals for forming the external connection terminals, the semiconductor device being connected to the mounting board through the bumps.

87. A semiconductor wafer on which semiconductor elements are provided, comprising: a semiconductor wafer 40 including a plurality of semiconductor elements having a surface on which protruding electrodes 44 are formed; and a compressed resin layer 43 which is formed on the surface of the semiconductor elements and seals at least a lateral surface of the protruding electrodes.

88. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 44 are formed; and a compressed resin layer 43, 61 which is formed on the surface on the semiconductor element and seals at least a lateral surface of the protruding electrodes, wherein a lateral surface of the resin layer and a lateral surface of the semiconductor element have planes cut by a dicer.

89. A semiconductor device as claimed in claim 88, wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have a common plane cut by a dicer.

90. A semiconductor device comprising: a semiconductor element having a surface on which external connection electrodes 44 are provided, which are to be electrically connected to external terminals; and a compressed resin layer 43 provided on the surface of the semiconductor elements so as to cover the external connection electrodes 44, wherein the external connection electrodes 44 are exposed at a lateral surface of the compressed resin layer, the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer.

91. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 44 are formed; and a resin layer 43 which is formed on the surface on the semiconductor element and seals a lateral surface and a top of the protruding electrodes, the resin layer slightly covering upper portions of the protruding electrodes, wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer.

97. The semiconductor device as claimed in claim 88, wherein the compressed resin layer is formed by disposing a film between the protruding electrodes and a mold, which thus contacts the sealing resin through the film.

98. The semiconductor device as claimed in claim 88, wherein a sheet-shaped resin is used as the sealing resin.

99. The semiconductor device as claimed in claim 88, wherein a reinforcement plate is loaded into a mold before the substrate is loaded onto the mold in forming the compressed resin layer.

100. The semiconductor device as claimed in claim 88, wherein: a film used in forming the compressed resin layer is formed of an elastically deformable substance, and the ends of the

protruding electrodes are caused to fall in the film when the resin layer is formed by using a mold; and the film is detached from the resin layer when the protruding electrode is exposed so that the ends of the protruding electrodes can be exposed from the resin layer.

101. The semiconductor device as claimed in claim 88, further comprising a heat radiating member 46 provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

To further clarify the teaching of a compressed resin layer 43, it is noted that Kata teaches this product at column 8, lines 23-24; and column 9, lines 37-43 because the resin layer is inherently compressed when the film is pressed.

To further clarify the teaching of a resin layer 43 which seals a top of the protruding electrodes, it is noted that the resin layer seals a top of the lateral surface of the electrode. In any case, there is no absolute frame of reference recited; therefore, it is inherent that for any particular sealed portion of the electrode, an absolute frame of reference can be chosen in which the portion is a top of the electrode.

To further clarify the teaching of the resin layer slightly covering upper portions of the protruding electrodes, attention is directed to figure 8D wherein the resin layer slightly covers the upper portions of the protruding electrodes that slightly overlap the external surface of the layer.

Also, although White does not appear to explicitly teach the process limitations of claims 97, 99 and 100, the product of White inherently possesses the structural characteristics imparted

by the limitations. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kata.

Kata is applied to the rejection as it is applied to the rejection of claim 18.

Kata does not appear to explicitly teach:

41. The semiconductor device as claimed in claim 18, wherein the resin layer comprises a plurality of resin layers having different characteristics.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to form the resin layer of Kata wherein the layer comprises a plurality of resin layers by splitting the step of forming the resin layer into a plurality of steps of forming a plurality of resin layers. Indeed, it has been held that the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, is prima facie obvious absent a disclosure that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical; Ex parte Rubin 128 USPQ 159. Furthermore, it is inherent in the resin layers so produced that the layers would have different characteristics. For example, they would each have a different characteristic of age and position.

Claims 54-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitahara (5568363).

At column 5, line 25 to column 16, line 34 Kitahara teaches the following:

54. A semiconductor device comprising: a semiconductor element 1; protruding electrodes ("circular-arc form") functioning as external connection terminals; a wiring board 4 having a flexible base 41 on which leads 3 are formed, the leads having ends 31 connected to the semiconductor element and other ends 32 connected to the protruding electrodes; and a sealing resin 2 sealing the semiconductor element, wherein there are provided extending portions 3 that are formed to the wiring board so that the extending portions laterally extend from a position in

which the semiconductor element is placed, the protruding electrodes being formed on the extending portions.

55. The semiconductor device as claimed in claim 54, further comprising a frame 95 which supports the wiring board and which has a cavity which accommodates the semiconductor element.

56. The semiconductor device as claimed in claim 54, wherein the protruding electrodes are mechanical bumps obtained by plastic deforming the leads.

Claims 79 and 81-83 are rejected under 35 U.S.C. 102(b) as being anticipated by McMahon (5362656).

At column 2, line 30 to column 4, line 27 McMahon teaches the following:

79. A semiconductor device comprising: a semiconductor device main body 14 having a semiconductor element having a surface on which protruding electrodes are directly formed, and a compressed resin layer 44 which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; an interposer 26 to which the semiconductor device main body is attached, a wiring pattern 30 to which the semiconductor device main body is connected being formed on a base member 28 of the interposer; an adhesive which is provided between the semiconductor device main body and the interposer and which bonds the semiconductor device main body to the interposer; a conductive member 40 which electrically connects the semiconductor device main body and the interposer; and external connection terminals 12 which are connected to wiring pattern through holes formed in the base member and

are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

81. The semiconductor device as claimed in claim 79, wherein the conductive member comprises stud bumps.

82. The semiconductor device as claimed in claim 79, wherein the conductive member comprises flying leads, which are integrally formed with the wiring pattern and bypasses the adhesive so as to be connected to the protruding electrodes.

83. The semiconductor device as claimed in claim 82, wherein connections of the protruding electrodes and the flying leads are sealed by resin.

Claims 88 and 97-100 are rejected under 35 U.S.C. 102(e) as being anticipated by White (5665655).

At column 3, lines 52-66; column 5, line 29 to column 6, line 22; column 6, line 65 to column 7, line 10; column 7, lines 36 to 50; column 8, lines 17-22; column 9, lines 38-42; and column 10, lines 19-25, White teaches the following:

88. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 6, 38 are formed; and a compressed resin layer 3, 36 which is formed on the surface on the semiconductor element and seals at least a lateral surface of the protruding electrodes, wherein a lateral surface of the resin layer and a lateral surface of the semiconductor element have planes cut by a dicer.

97. The semiconductor device as claimed in claim 88, wherein the compressed resin layer is formed by disposing a film between the protruding electrodes and a mold, which thus contacts the sealing resin through the film.

98. The semiconductor device as claimed in claim 88, wherein a sheet-shaped resin is used as the sealing resin.

99. The semiconductor device as claimed in claim 88, wherein a reinforcement plate is loaded into a mold before the substrate is loaded onto the mold in forming the compressed resin layer.

100. The semiconductor device as claimed in claim 88, wherein: a film used in forming the compressed resin layer is formed of an elastically deformable substance, and the ends of the protruding electrodes are caused to fall in the film when the resin layer is formed by using a mold; and the film is detached from the resin layer when the protruding electrode is exposed so that the ends of the protruding electrodes can be exposed from the resin layer.

Although White does not appear to explicitly teach a compressed layer, it is inherent that the layers would be compressed by atmospheric pressure, the weight of themselves and the overlying layers, and by the dicing process.

Also, although White does not appear to explicitly teach the process limitations of claims 97, 99 and 100, the product of White inherently possesses the structural characteristics imparted by the limitations. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claim 102 is rejected under 35 U.S.C. 103(a) as being unpatentable over White as applied to claim 88, and further in combination with Cole (5434751).

Although White teaches that the resin layer comprises a plurality of dielectric layers including polyimide resin or other dielectric material, White does not appear to explicitly teach that the layer comprises a plurality of resins having different characteristics. Regardless, at column 6, line 34, to column 7, line 41, Cole teaches an "ULTEM" resin dielectric layer. Moreover, it would have been obvious to combine the product of Cole with the product of White because it would provide a dielectric layer.

Claims 70, 72-77, 80, 84, 85, 95 and 96 are allowed.

Applicant's amendment and remarks filed 8-7-00 are adequately addressed by the rejection supra.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist at (703) 308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m..

The fax phone number for group 2800 is (703)305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.